REMARKS.

By this amendment, claims 40 and 48 have been amended to clarify and make more explicit certain recitations therein. New claims 62-65 have been added. No claims have been cancelled and no new matter has been added. Consideration taking into account the following remarks is respectfully requested.

Note has been taken of the assertion in the Office Action that the relevant consideration for allowance of the claims under rejection is the patentability of the structure resulting from the processing steps recited in the claims. On behalf of the applicants, it is again asserted that all of the claims under rejection, as well as the newly added claims, are indeed directed to structures that are novel and patentable over the cited references, for reason as set forth in the response filed April 3, 2000 in addition to the following reasons.

Post fabrication deuterium passivation, as claimed in the claims pending in this application, accumulates deuterium both at the channel-gate oxide and gate contact-gate oxide interfaces mainly from the drain and source sides, as well as from above at the drain contact - silicon and source contact-silicon interfaces. The location and distribution of deuterium in this manner is a distinctive structural characteristic of and detectable in the end product resulting from carrying out the process steps as claimed in this application. That product is structurally differentiated from and patentable over the product resulting from Lisenker and Saks cited in the Office Action, in both of which deuterium treatment is carried out before contact formation, and has important advantages over the products resulting from the processes disclosed by those two references. The rejection of claims 40-48 and 60-61 is respectfully traversed.

Lisenker explicitly teaches deuterium annealing during fabrication process steps (see for example, page 8, line 29 to page 9, line 4), such as doping, etching, annealing, deposition, cleaning, passivation and oxidation steps, particularly emphasizing the importance of deuterium annealing *"in those fabrication steps in which a permanent oxide layer is being*

formed or treated" (page 8, lines 35-37) as contrasted with post fabrication deuterium treatment as required by claims 40-48 and 60-65 of this application.

Saks discloses deuterium treatment during fabrication of a MOSFET structure, in which *"[t]he annealing was performed after diffusion of the polysilicon gates and implantation of the N+ source/drains. This anneal was the last high-temperature (> 500°C) fabrication step. No subsequent high temperature processing steps were allowed in order to prevent diffusion of the . . . deuterium back out of the oxide which happens above 500°C . . .."* (page 2221, left column, lines 27 - 33).

However, in a more recent 1999 paper *"Process Stability of Deuterium-Annealed MOSFET's"*, W.F. Clark et al, IEEE Electron Device Letters, Vol. 20, No. 1, January 1999, IBM Microelectronics Division workers reported on the process stability of deuterium-annealed MOSFETs using various types of anneal and anneal conditions for different groups of MOSFETs. Clark et al reported *inter alia,* that *"NMOSFET's from groups C, D, and E were annealed following silicide formation and prior to any silicon nitride or PSG deposition"* (page 48, right column, lines 35-37) i.e. <u>not</u> post fabrication treatment after contact formation. As shown in Table I (page 49) of Clark et al report that MOSFET samples C1, C3, C6, D1 (page 89, lines 37-39) were subjected to an annealing atmosphere containing deuterium. Referring to the Results Summary column in Table I for deuterium treated samples C1, C3, C5, D1, improvement in device lifetime is indicated - but this is <u>prior</u> to any subsequent fabrication steps, including contact formation.

Samples from E1 and E2 were subjected to post silicide deuterium annealing (Table 1, Group E) and *[s]everal of these post-silicided annealed wafers (E1) were processed to first metal, including an intermediate silicon nitride and PSG deposition. At first metal stress, no hot-carrier improvement was observed. . . SIMS analysis for the 10% deuterium anneal sample without subsequent processing (E1) is given in Fig. 3. The deuterium profile indicates low signal in the silicide with concentrations between 10^{18} and 10^{19} atoms/cm^3 in the polysilicon and gate oxide regions. . . . <u>Samples from cell E1 were then subjected to a</u>*

relatively low-temperature silicon-nitride deposition of 480°C for 2min. (E2); the SIMS analysis is included in Fig. 3 and shows that the deuterium present at the post-silicide has migrated away from the Si/SiO2 interface region. . . . [T]he peak observed at the nitride/silicide interface [E2] *is not present in the deuterium profile of the control sample* [E1]. *Evidently, this peak is related to the migration of deuterium from the Si/SiO2 interface regions. Clearly, the nitride cap processing is sufficient to modify the deuterium distribution in the films* (paragraph bridging pages 49 and 50). Clark et al conclude *"We can improve NMOSFET hot-carrier lifetime at an earlier stage in the semiconductor process flow by annealing the transistor prior to silicon-nitride deposition. The increased device lifetime observed with nitride gate oxides are further improved with deuterium anneals. The benefit of the deuterium anneal, however, is inherently unstable with further wafer processing."* (Page 50, III. CONCLUSION.) (Underlining added for emphasis.)

From this analysis by Clark et al, it can be seen that Saks hypothesis that processing above 500°C subsequent to deuterium annealing should be avoided is incomplete and that subsequent processing at lower temperatures can effectively deplete deuterium from the deuterium annealed region(s), so that contact formation subsequent to deuterium annealing, typically requiring temperatures above 400°C, would result in deuterium migration from the Si/SiO2 interface regarded as a critical location for deuterium by both Lisenker and Saks.

It may thus readily be concluded that a device as defined in any of claims 40-65 has a structure that is differentiated from a structure produced by the fabrication methods taught by Lisenker and Saks. Clark et al have shown that, post fabrication, the deuterium at the silicon/ silicon dioxide interface due to the earlier annealing process, will no longer effectively remain because of the higher temperature processing, subsequent to the deuterium annealing, required to form contacts to the MOSFET structures of Lisenker and Saks.

A device as claimed in any of claims 40-65, is *"structurally characterized by the presence of deuterium at said interface [between a semiconductive silicon layer and a gate oxide layer] resulting from post-fabrication passivation of said interface in a heated, deuterium gas-enriched atmosphere"* (claim 1) and retains deuterium at that interface to effect the recited passivation. This, is indeed a structural differentiation from both Lisenker and Saks, neither of which, as evidenced by Clark et al, discloses or suggests a process that results in the production of such a structure. Neither Lisenker nor Saks et al suggests post fabrication deuterium passivation and consequently the resultant novel structure cannot be rendered unpatentable by either of those references.

Claims 48 and 62 explicitly specify *"said post fabrication passivation is carried out after formation of said conductive contacts and produces a structure including covalently-bound deuterium populating said [interface between a semiconductive silicon layer and a gate oxide layer]"* (claim 48) and *"said semiconductive device structurally characterized by post-fabrication heating of the device after formation of said contacts, in a deuterium gas-enriched atmosphere . . . to provide deuterium at and to passivate said interface"* (claim 62). See applicant's specification, page 12, lines 10-12. As shown in the above discussion, Clark et al demonstrate that no such structures, with completed contacts to the source, drain and gate regions, result from the process teachings of Lisenker or Saks.

Further structural advantages of a device as claimed in claims 40-65, is that post-fabrication deuterium processing results in the location of deuterium not only at the channel-gate oxide but also at the gate contact-gate oxide interface, in both locations by diffusion mainly from the drain and source sides, as well as from above at the drain contact - silicon and source contact-silicon interfaces. The enhanced location of deuterium at this region of the silicon-gate oxide interface neighboring the drain contact, is advantageous as is evidenced by D. J. DiMaria (IBM Thomas J. Watson Research Center) in *Defect generation in field-effect transistors under channel-hot-electron stress,* Journal of Applied Physics, Vol. 87, Number 12, pp. 8707-8715, 15 June 2000, showing that hot electron damage at the silicon-gate oxide interface occurs close to the drain contact (p. 8713, last four lines,

continuing through p. 8713, right column, line 5 and Fig. 12). The location of deuterium in this region in a device structure as claimed in the claims of this application, is thus independently shown to be particularly effective in relieving the results of such hot electron damage. No such deuterium accumulation is present, post fabrication, in devices treated as taught by Lisenker or Saks, in which deuterium treatment is taught as having been carried out prior to contact formation, so that as evidenced by Clark et al, deuterium will have migrated and not be effectively present in the post contact structure. Consequently, the invention as recited in claims 40-65 is structurally differentiated from Lisenker and Saks.

The assertion in the Office Action "*. . . it would have been obvious . . . to define the practical lifetime of the Lisenker et al* [p3] (or *Saks et al* - p.4*) device because this is well known in the art"* is not understood. It appears the relevant issue is not "defining" a lifetime, but whether or not a device produced by Lisenker or Saks has such a lifetime characteristic and this has not been shown in the Office Action to be the case. Accordingly, to the extent it may be pertinent, these assertions in the Office Action are respectfully traversed.

Patent 6,023,093 (Gregor) cited but not relied on has been noted but comment thereon is not seen to be required.

An Information Disclosure Statement accompanies this amendment, formally bringing to the attention of the Examiner, as material to examination of this application, the later published Clark et al and DiMaria publications referred to above. Consideration and entry into the record of the Clark et al and DiMaria publications is requested.

It is believed this amendment and the accompanying remarks have addressed all outstanding grounds of rejection, demonstrated that the claimed invention is patentable over the references of record, and that all of claims 40-48 and 60-65 are in condition for allowance. Early action to that effect will be appreciated.

If after consideration, the Examiner believes that further prosecution of the application may be facilitated by discussion, a telephone call to the undersigned attorney at 972-490-3695 will be appreciated.

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